ABSTRACT OF THE DISCLOSURE

A device interface circuit unit transfers a command and data in packet format between the unit and the host. A transport layer is provided with a receive FIFO, a command detection circuit and a send FIFO, and an application layer is provided with a receive task file register and a send task control file register. An available time is generated for each break point of a packet during data transfer in order to receive another command packet from the host. When the command packet is received from the host in the available time during data transfer, the data transfer is suspended and the received command is decoded to execute a process for continuing or canceling the data transfer, after which the data transfer is resumed.